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RESEARCH ARTICLE

Fabrication and Electrical Characterization of Two-dimensional Atomic-layer-thick MoS_2 Field Effect Transistors

Seungyeon Lee

Bishop Montgomery High School, 5430 Torrance Blvd, Torrance, CA 90503, USA; beckyleesy@gmail.com

ABSTRACT: Two-dimensional (2D) transition metal dichalcogenides have emerged as promising channel materials for next-generation electronic devices due to their atomic-scale thickness and excellent electrical properties. In this work, I report the fabrication and electrical characterization of field-effect transistors (FETs) based on atomic-layer-thick molybdenum disulfide (MoS_2). Few-layer MoS_2 flakes were mechanically exfoliated and transferred onto Si/SiO_2 substrates, followed by standard lithographic patterning of the source and drain electrodes. The fabricated MoS_2 FETs exhibit typical n-type conduction behavior with a clear gate modulation. Key device parameters, including on-off current ratio, threshold voltage, and mobility, were extracted and analyzed. The results demonstrate the suitability of 2D MoS_2 as a promising material for future nanoscale electronic applications.

KEYWORDS: Engineering, Electronics, Two-dimensional Semiconductor, MoS_2, Field Effect Transistor.

Introduction

A transistor is a core electronic component that uses semiconductors to switch on and off by controlling the flow of current, and it is the fundamental element that powers modern electronic devices, including logic circuits and memory. In the semiconductor industry, the number of transistors on an integrated circuit has doubled approximately every two years for decades.1 This trend has led to increasing computing power, smaller devices, and lower costs. However, this development faces physical limits as transistors approach atomic sizes. Recently, two-dimensional (2D) nanosheets acting as ultrathin films have gained significant interest for use in the miniaturization of electronic devices to the atomic-layer thick scale. Graphene, an atomic-thick sheet composed of carbon atoms, is a 2D material known for its high tensile strength, electrical conductivity, and transparency.[2] However, graphene cannot be used as an active channel in transistors because it is a zero-bandgap material or a semi-metal.[2]

On the other hand, molybdenum disulfide (MoS_2), a transition metal dichalcogenide semiconductor, has attracted considerable attention. Unlike graphene, MoS_2 has a band gap of ~1.2 eV in bulk and ~1.8 eV in a monolayer.[3] MoS_2 has a layered structure composed of S-Mo-S units bonded by van der Waals forces, and it can also be formed into atomic-layer films because individual layers can be peeled off using mechanical exfoliation.[2,3]

Here in this study, I report on the fabrication and electrical characterization of MoS_2 field-effect transistors. The MoS_2 flakes were prepared by a mechanical exfoliation method on Si substrates. Transistor devices were then fabricated with a few layers of MoS_2 nanosheets by lithography processes, and their electrical properties were characterized.

Experiments:

Molybdenum disulfide (MoS_2) is a transition metal dichalcogenide compound known for its layered structure, high electrical mobility, and tunable bandgap.[2] Figure 1 shows the structure of MoS_2 viewed from three different directions. MoS_2 has a stacked structure of weakly bonded layers with van der Waals forces between the layers. The spacing distance of MoS_2 layers is 0.65 nm.[3] The monolayer MoS_2 can be formed by mechanically exfoliating MoS_2 crystals in a similar method to forming graphene.

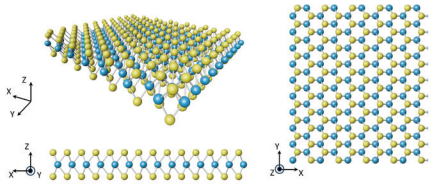

Figure 1: The structure of MoS_2 viewed from three different directions. MoS_2 has a stacked structure of weakly bonded layers. Images drawn using Blender, a 3D creation software.

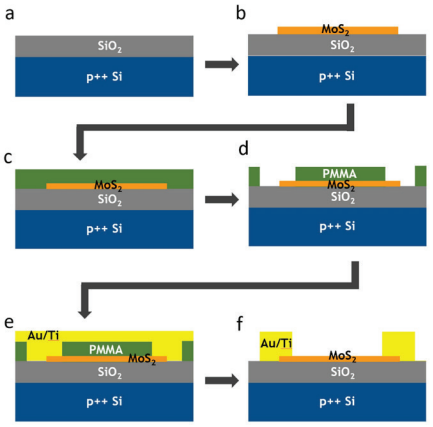

Figure 2: Schematic illustration of MoS_2 transistor device fabrication. (a) Si substrate. (b) MoS_2 flake transferred on substrate. (c) PMMA coating. (d) Pattern development in PMMA. (e) Metal deposition. (f) Lift-off to form electrodes.

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Figure 2 illustrates the fabrication processes of the MoS2 field effect transistors (FETs). The substrates are pieces of Si wafer that are composed of 270 nm SiO_2 as gate dielectric on a highly doped p++ Si as back gate (Figure 2a). MoS_2 flakes are transferred from a MoS_2 bulk crystal by a scotch tape exfoliation method (Figure 2b). To make patterns of electrodes, poly(methyl methacrylate) (PMMA) is spin-coated over the sample pieces at a rate of 4000 rpm for 50 s (PMMA film thickness of ~350 nm) (Figure 2c). PMMA is a standard positive resist used in electron beam lithography, enabling high-resolution patterns to be created because exposure to the electron beam breaks the polymer bonds in PMMA and dissolves the areas of PMMA exposed to the electron beam. After the spin-coating of PMMA, the substrates are baked on a hot plate at 180 °C for 90 s. The electrode regions in the PMMA layer are then patterned using an electron beam lithography system (JSM-6510, JEOL) with a 30 kV exposure (Figure 2d). The pattern development was performed with a methyl isobutyl ketone: isopropyl alcohol (MIBK: IPA) (1:3) solution with a development time of 50 s. For electrodes, Au (50 nm thick) and Ti (5 nm thick) are deposited by an electron beam evaporator (Figure 2e). The lift-off process removes unnecessary Au/Ti layers to define the source and drain electrodes, and the transistor devices are completed (Figure 2f).

Figure 3 shows a series of optical images during the device fabrication processes. Figure 3a is the optical image of a SiO_2/Si substrate. The substrates have pre-designed alignment marks for the purpose of locating MoS_2 flakes (Figure 3a). The transferred MoS_2 flakes on the substrates are imaged and examined by optical microscopy (Figure 3b). Figures 3c-3e show sequential images of samples during the device fabrication. Images were taken after MoS2 flakes were transferred onto the substrate (Figure 3c), after patterns were developed for electrodes in a spin-coated PMMA layer (Figure 3d), and after MoS_2 FETs were fabricated with the source and drain electrodes (Figure 3e).

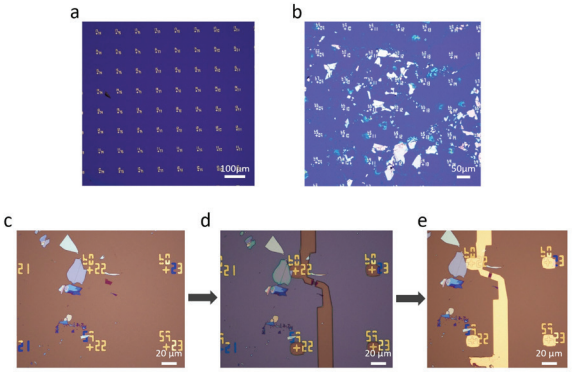

Figure 3: Optical images during the device fabrication processes. Optical images of (a) a SiO_2/Si substrate and (b) transferred MoS_2 flakes on the substrate. (c-e) Sequential images of samples during the device fabrication. Optical images (c) after MoS_2 flakes are transferred on the substrate, (d) after patterns are developed for electrodes, and (e) after MoS2 FETs are fabricated with the electrodes.

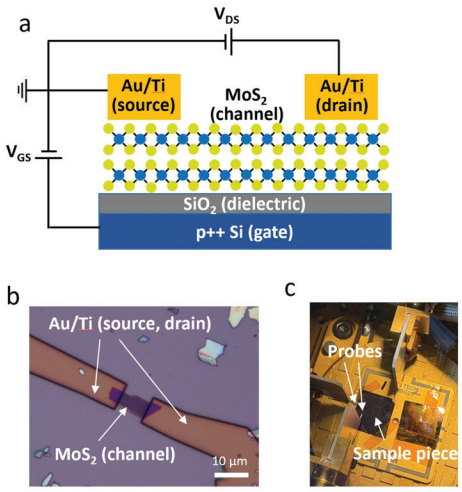

Figure 4: (a) MoS_2 FET device structure. (b) Optical image of a completed device. (c) Optical image of a device sample in the probe station.

Figure 4a shows a schematic of the completed MoS2 transistor device structure, including electrical circuit connections. The current flow between the source and drain electrodes is measured while voltages are applied with the source electrode grounded. Figure 4b shows an optical image of a fabricated transistor with a MoS2 channel contacted with source and drain electrodes. Then, the electrical characteristics of the fabricated MoS2 FETs are measured using a semiconductor parameter analyzer (Keithley 4200 SCS) in a probe station (JANIS Model PS-100) in vacuum. Figure 4c shows a photographic image of the device sample pieces on a chuck in the probe station.

Results and Discussion

Figure 5 shows the optical images of three MoS_2 FET devices with the measured electrical data. Figures 5b and 5c are the electrical data for the device (Device 1) shown in Figure 5a, Figures 5e and 5f are the electrical data for the device (Device 2) shown in Figure 5d, and Figures 5h and 5i are the electrical data for the device (Device 3) shown in Figure 5g. Figures 5b, 5e, and 5h are output curves (I_{DS}–V_{DS}), i.e., the current flow between the drain and source electrodes (I_{DS}) while variable voltages are applied between the drain and source electrode (V_{DS}) with a fixed voltage applied between the gate and source electrodes (V_{GS}). Specifically, variable VDS from -1 V to 1 V with a step of 0.05 V and fixed V_{GS} (60, 40, 20, 0, -20, -40, or -60 V) were applied. Figures 5c, 5f, and 5i are transfer curves (I_{DS}–V_{GS}), i.e., the current flow between the drain and source electrodes (I_{DS}) while variable voltages are applied between the gate and source electrode (V_{GS}) with a fixed voltage applied between the drain and source electrodes (V_{DS}). Specifically, variable V_{GS} from 60 V to -60 V with a step of 1 V and fixed V_{DS} (1 or -1 V) were applied. For all the measured devices, the IDS increases as the V_{GS} increases positively, indicating that the MoS_2 FETs function as an n-type device, which means that electrons are the major charge carriers. This agrees with previous studies on MoS_2 FETs reported by others.[3,4] For a p-type device where holes are the major charge carriers, the I_{DS} would increase as the V_{GS} increases negatively. The device

performances of FETs are estimated by parameters such as on-off current ratio, threshold voltage, mobility, and subthreshold swing values, etc. The on-off ratio is the ratio of maximum on-state current to minimum off-state leakage current, and the threshold voltage (*Vth*) is the minimum gate voltage required to create an accumulation channel, enabling the device to switch from off-state to on-state. The mobility (μ) measures how quickly charge carriers move through the channel under an electric field, and the subthreshold swing measures the gate voltage required to change the drain current by one order of magnitude. Among these device parameters, I characterized the on-off ratio, threshold voltage, and mobility values for the three devices, as summarized in Table 1. These values are similar to those previously reported for MoS_2 FETs by others, which indicates that the devices were successfully fabricated and characterized in this study.[3,4]

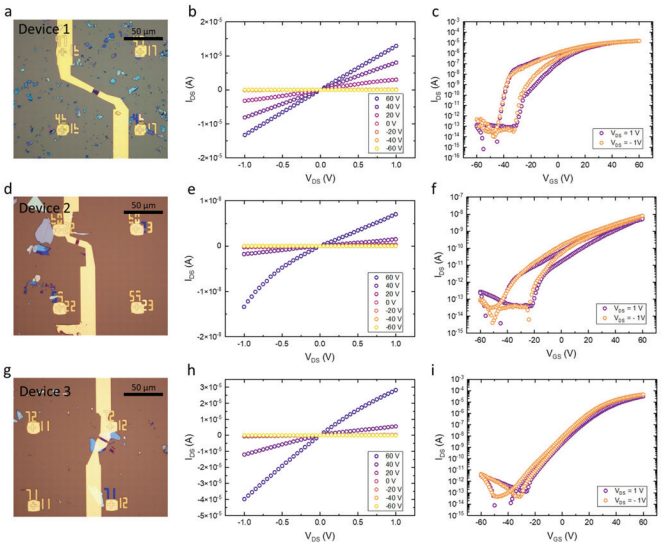

Figure 5: Optical images and electrical data of three MoS_2 FET devices. (a-c) Device 1, (d-f) Device 2, and (g-i) Device 3. (a,d,g) Optical images of devices. (b,e,h) Output curves (I_{DS}–V_{DS}) showing the current as a function of drain voltage. (c,f,i) Transfer curves (I_{DS}–V_{GS}) showing the current as a function of gate voltage. All the devices show that the current (I_{DS}) increases as the gate voltage (V_{GS}) increases positively, indicating that the MoS_2 FETs function as an n-type device, which means that electrons are the major charge carriers.

In particular, the on-off ratio was observed to be in the range of 10^6 to 10^9, while the off-state leakage current fell within the 10^{-13} A range. Note that Device 2 showed a particularly low current level, on-off ratio, and mobility values compared with those of Device 1 and Device 3, which suggests that Device 2 performs worse than the other two devices, which may be due to manufacturing flaws such as in PMMA coating, electron beam exposure, or metal lift-off, but the exact cause is difficult to determine.

The operation of MoS_2 FETs can be explained in the energy band diagrams shown in Figure 6. Figure 6a shows the diagram at V_{DS} = 0 and V_{GS} = 0 V. Figures 6b and 6c show the diagrams at non-zero V_{DS} with V_{GS} > 0 V and V_{GS} < 0 V, respectively. In particular, the Fermi level (E_F) of MoS_2 is closer to the conduction band minimum (E_C) than to the valence band maximum (E_V), which tells that MoS_2 is an n-type semiconductor (Figure 6a). When a positive V_{GS} is applied, the energy band of MoS_2 shifts down relative to E_F, and E_F becomes closer to E_C, resulting in a higher charge (electron) concentration in MoS_2 and more current flow between the source and drain electrodes (Figure 6b). And, when a large positive V_{GS} is applied, the device turns on, as shown in Figure 5. On the other hand, when a negative V_{GS} is applied, the energy band of MoS_2shifts up relative to E_F and E_F becomes farther away from E_C, resulting in a lower charge (electron) concentration in MoS_2 and less current flow between the source and drain electrodes (Figure 6c). And, when a large negative V_{GS} is applied, the device turns off, as shown in Figure 5.

Table 1: Summary of the device parameters (on-off ratio, threshold voltage, and mobility) extracted from the three measured devices.

	On-off ratio	V_{th} (V)	μ (cm²/V·s)
Device 1	10^8	13.5	6.0
Device 2	10^6	38.0	0.1
Device 3	10^9	34.8	4.0

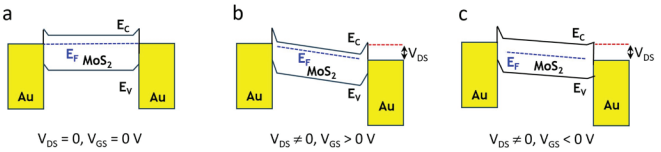

Figure 6: Energy band diagrams of MoS_2 FET under voltages at (a) V_{DS} = 0 and V_{GS} = 0 V, (b) non-zero VDS and V_{GS} > 0 V, and (c) non-zero V_{DS} and V_{GS} < 0 V. (b) The application of a positive V_{GS} increases the electron concentration within the MoS_2 channel, leading to enhanced current conduction and transitioning the device to the on-state. (c) A negative V_{GS} depletes the electron concentration, suppressing current flow and transitioning the device to the off-state.

Conclusion

MoS_2 FETs were successfully fabricated using mechanically exfoliated few-layer MoS_2 flakes transferred onto Si/SiO_2 substrates and patterned through standard lithographic processes. The resulting devices exhibited a clear n-type conduction behavior with effective gate modulation, confirming proper transistor operation. Key electrical parameters, including on-off current ratio, threshold voltage, and mobility, were systematically extracted to evaluate device performance. The research of 2D semiconductors is significant because their atomic-scale thickness allows for ultra-scaled electronic devices. Future research is expected to focus on achieving large-scale, defect-free synthesis technologies that ensure industrial-level reliability.

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Author

Seungyeon Lee is currently a junior at Bishop Montgomery High School in Torrance, California. Born in Korea, she moved to the United States in August 2023. She likes studying science.